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January 27th, 2000

PCI Performance
Guidelines and Measurements

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Innovating the HP Way

Objectives

At the end of this presentation you will:

- Know the measures needed to make gross comparisons between PCI devices
- Understand why a device has a particularly good or bad performance
- Understand what is required to improve performance
- Understand the tools needed to make make the measurements and interpret results

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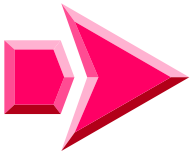
Content



- Motivation
- PCI Measures for Device Comparisons
- Examples
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- Real-time vs. Post Processed Measurements
- Recommendations and Conclusions

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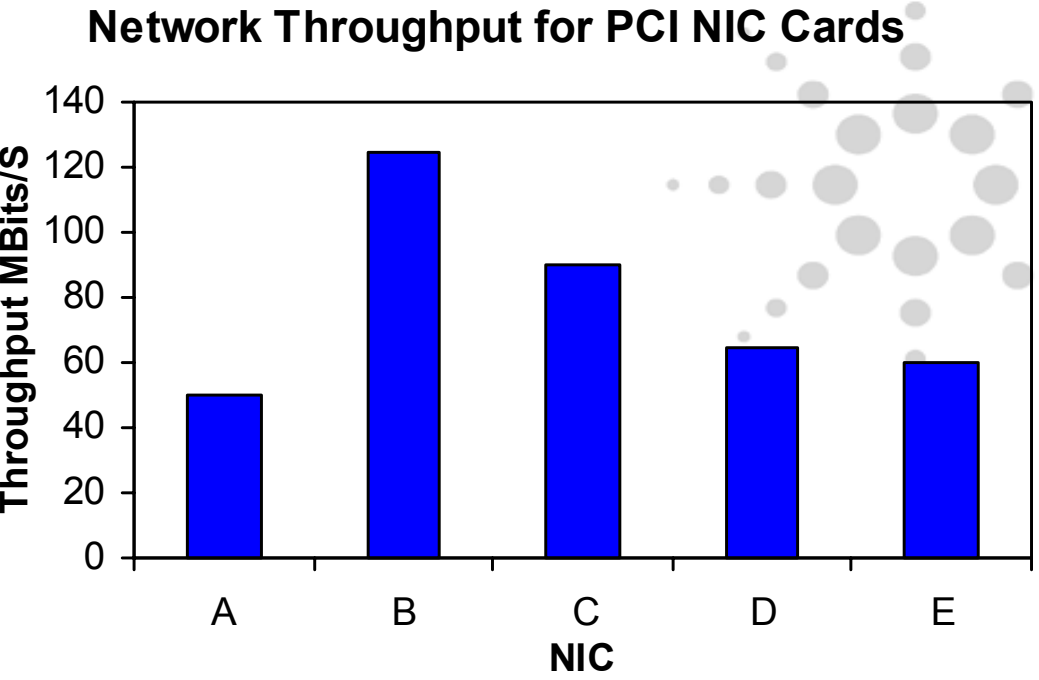
Performance - the driving force

- Performance: most important criteria for end users to buy a new computer or a new I/O device

- One slow device in a system degrades the performance of the entire system

Network Interface Card Comparison

All PCI Devices are NOT made Equal!!!



- 5 Network Interface cards from 5 independent vendors
- Network Benchmark
- Same system

From Efficient Use of PCI by Platform Architecture Labs - Intel Corporation

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Performance - important for high reliability and usability

- Better performance
  - ⇨ better handling of high load situations
- Non real-time operating systems need fast systems to get everything done in time
- A slow system is no fun to work with

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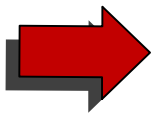
System Integrator's Need a Measure to Compare Devices

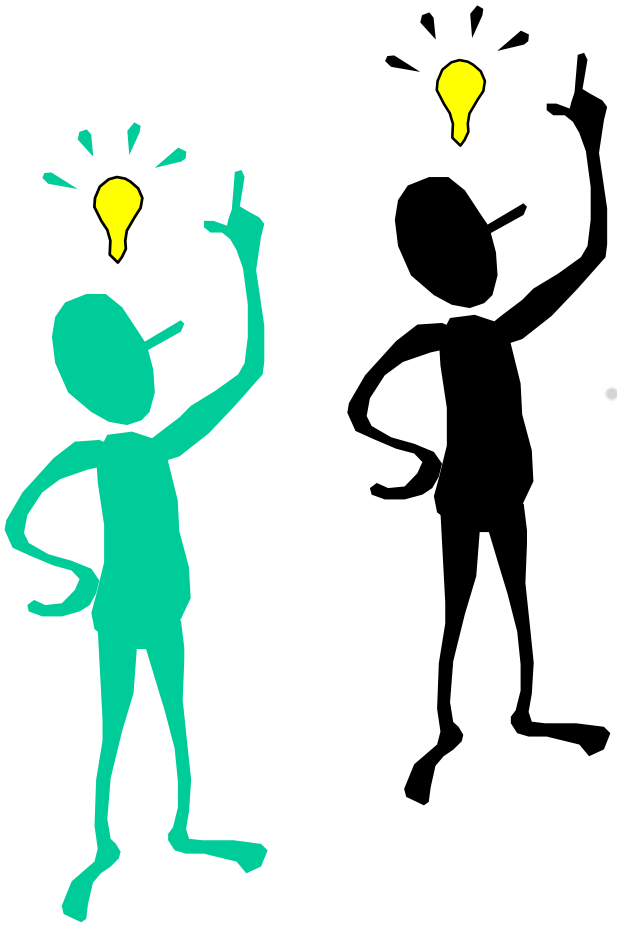
- System Integrators need a fast and consistent decision criteria to distinguish between "good" and "bad" devices for their system.

- Devices must be "good team player" or "good citizen" on the bus.



Efficiency

Efficiency



- How well your device uses the bandwidth it gets from the system.
- Improving efficiency frees system resources and avoids bottlenecks.
- Good efficiency speeds up an application only in high load situations.

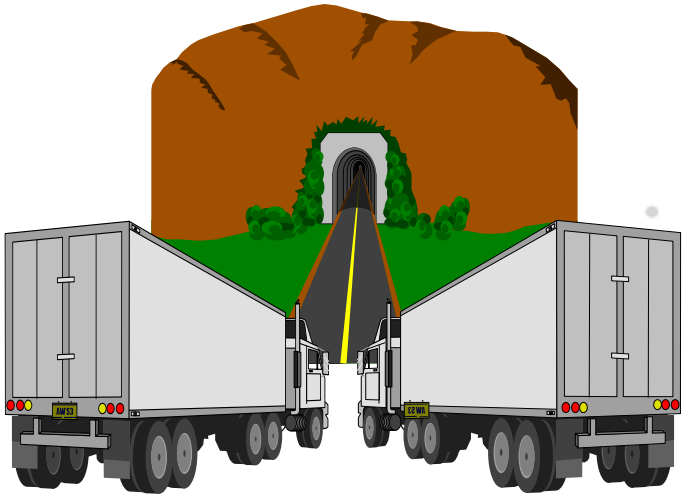
Definition of Efficiency

$$E = \underbrace{\text{Time Efficiency}}_{\frac{\text{Number of data cycles}}{\text{Number of used cycles}}} * \underbrace{\text{Byte Enable Efficiency}}_{\frac{\text{Number of transferred bytes}}{\text{Number of data cycles} * 8}}$$

Any clock where FRAME#, IRDY#, TRDY#, DEVSEL# or STOP# is low.

Maximum number of transferable bytes per clock (4 in 32 bit systems).

Throughput



- PCI provides up to 528 Mbytes/sec (64 Bit, 66 MHz).
- Applications require a certain throughput.
- Measured as a % of theoretical maximum or in Mbytes/sec

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Definition of Throughput

$$T = \frac{\text{Number of transferred bytes}}{\text{Total Number of clocks} * 8} \times 100\%$$

Maximum number of transferable bytes per clock (4 in 32 bit systems).

Definition of Utilization

Any clock where FRAME#, IRDY#, TRDY#, DEVSEL# or STOP# is low.

$$U = \frac{\text{Number of used cycles}}{\text{Total Number of cycles}}$$

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Measurement Example on PCI

Idle
Address Phase
Decoding
Wait
Wait
Wait
Data Transfer with 4 Bytes
Wait
Data Transfer with 4 Bytes
Idle

Efficiency = 25 %

- 2 out of 8 busy clocks are data

Utilization = 80 %

- 8 out of 10 clocks are busy

Throughput = 20 %

- 2 out of 10 clocks are data

T/P = Efficiency * Utilization

Example Relating Efficiency/Throughput/Utilization

Application Needs this throughput	Efficiency of Transactions	Resulting Utilization	Effect of adding a 2nd device
13 Mb/s (10% of 133)	50% (Good)	20% of bus	No effect
13 Mb/s (10% of 133)	20% (Bad)	50% of bus	Slow down, Or hang

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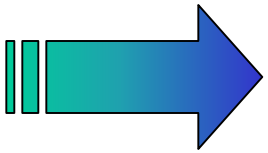
Efficiency - the most important measure in PCI Performance

PCI Efficiency is exactly the measure the system integrator needs.

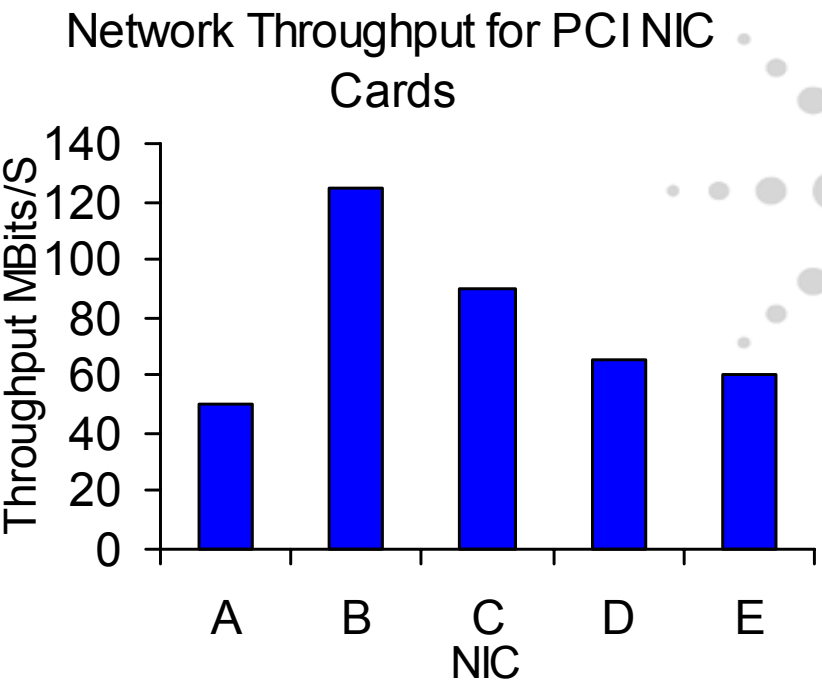
Chip set developer and Add-In card manufacturer are primarily interested in the throughput they need for their application.

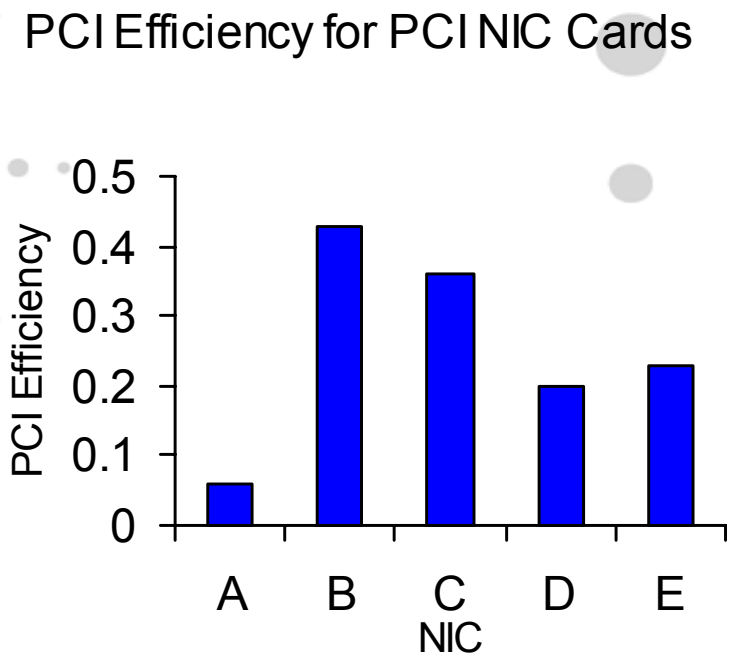


But they need to optimize for efficiency also because they need to share PCI bandwidth

NIC Card Comparison

All PCI Devices are NOT made Equal!!!





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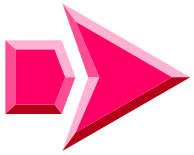

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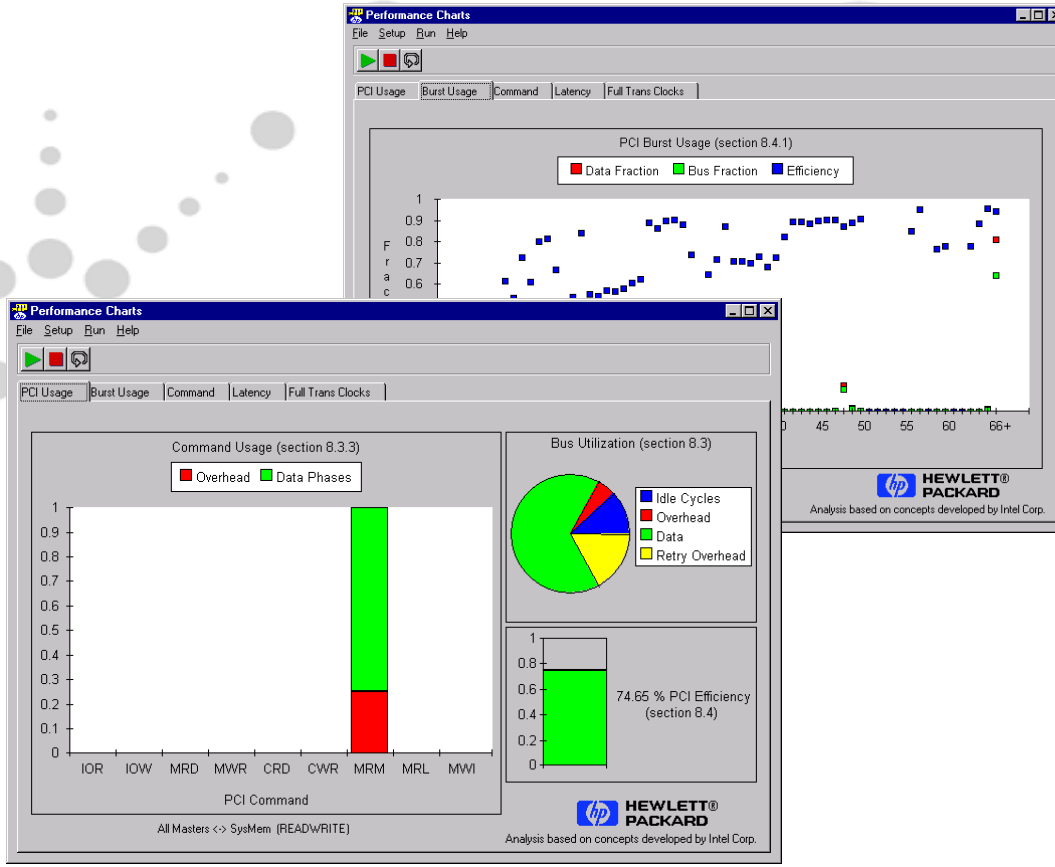
Measurements for Optimization

Determining the root cause of poor performance:

- Non-retry Efficiency and Utilization
- Command Usage
- Burst sizes
- Latencies
- Who is the bottleneck?
- And many more...



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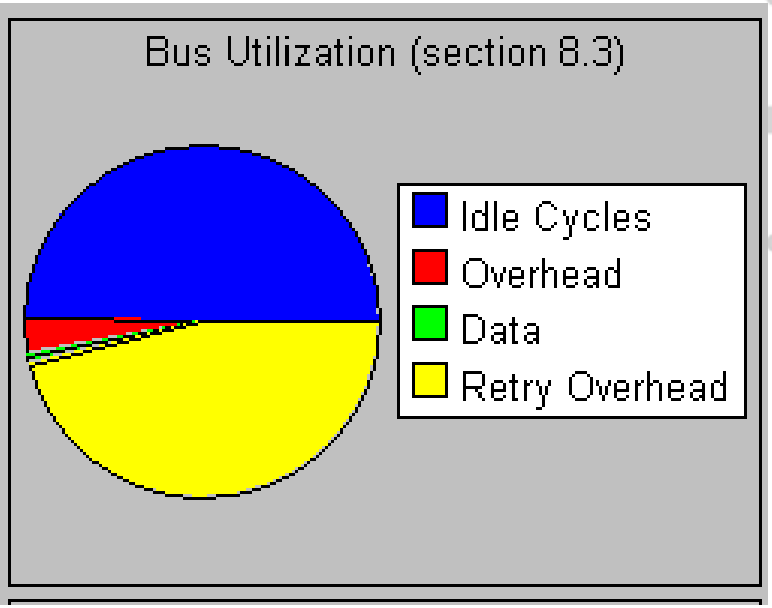
Non-retry Efficiency and Utilization

- Needed to compare high and low load conditions

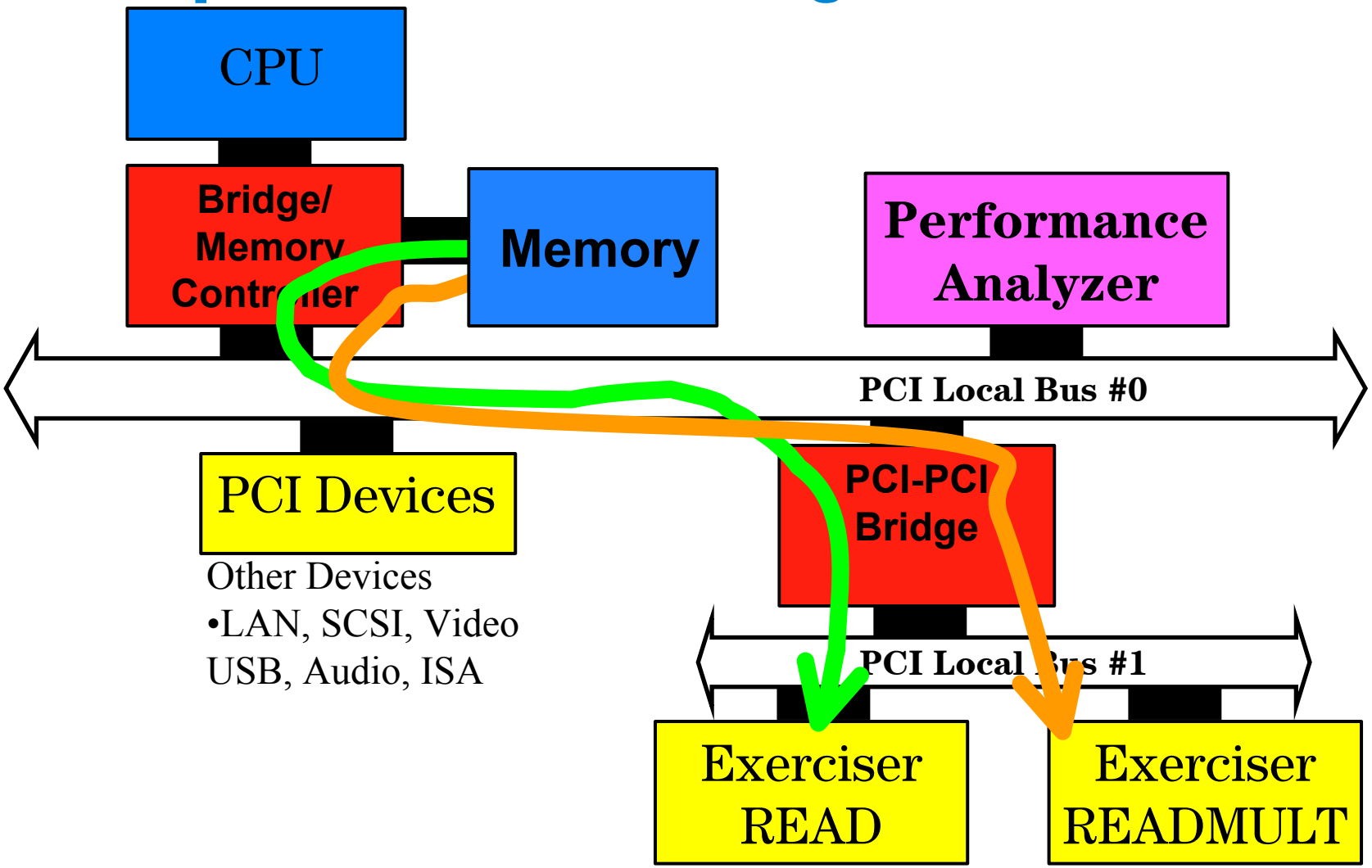
Bus Utilization



Report Output

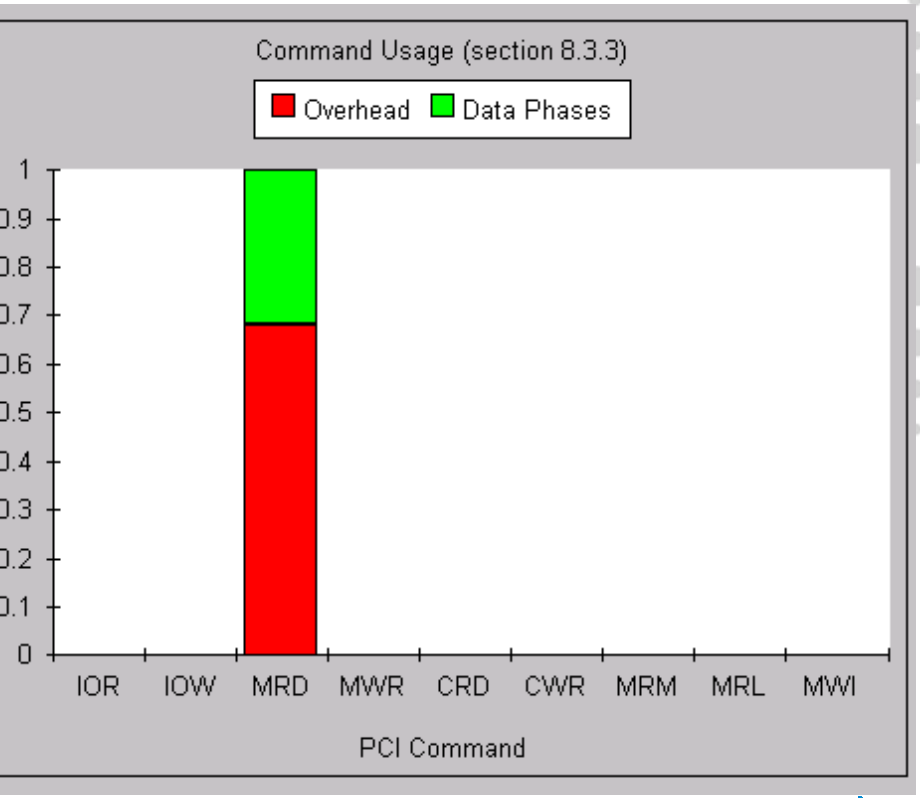
```
PCI Utilization                51.2 %
Non-retry PCI Utilization       6.6 %

PCI Efficiency                  1.7 %
Non-retry PCI Efficiency       11.4 %
```

Example - Command Usage (1)

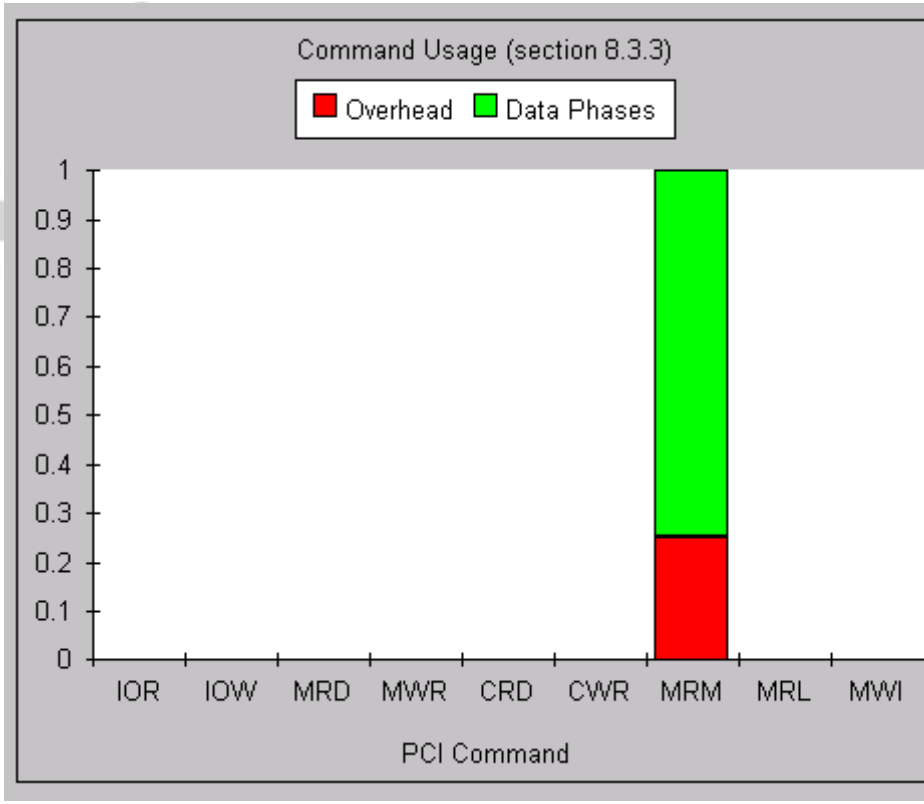


Example - Command Usage (2)

Memory Read Command

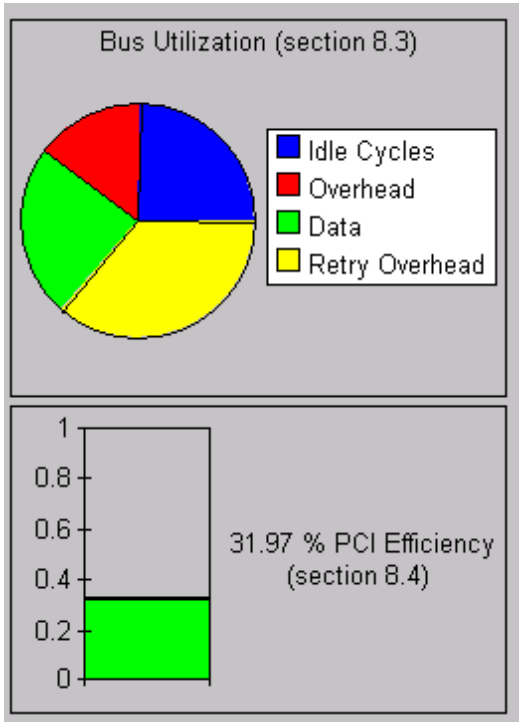


Memory Read Multiple Comman



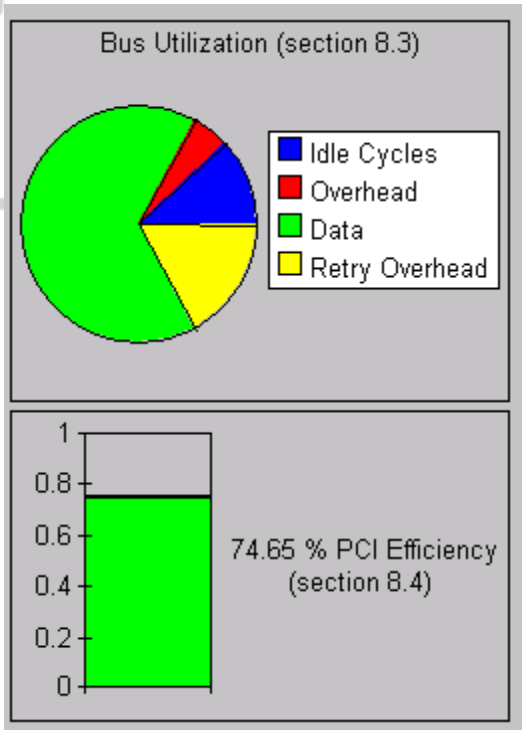
Example - Command Usage (3)

Memory Read Command



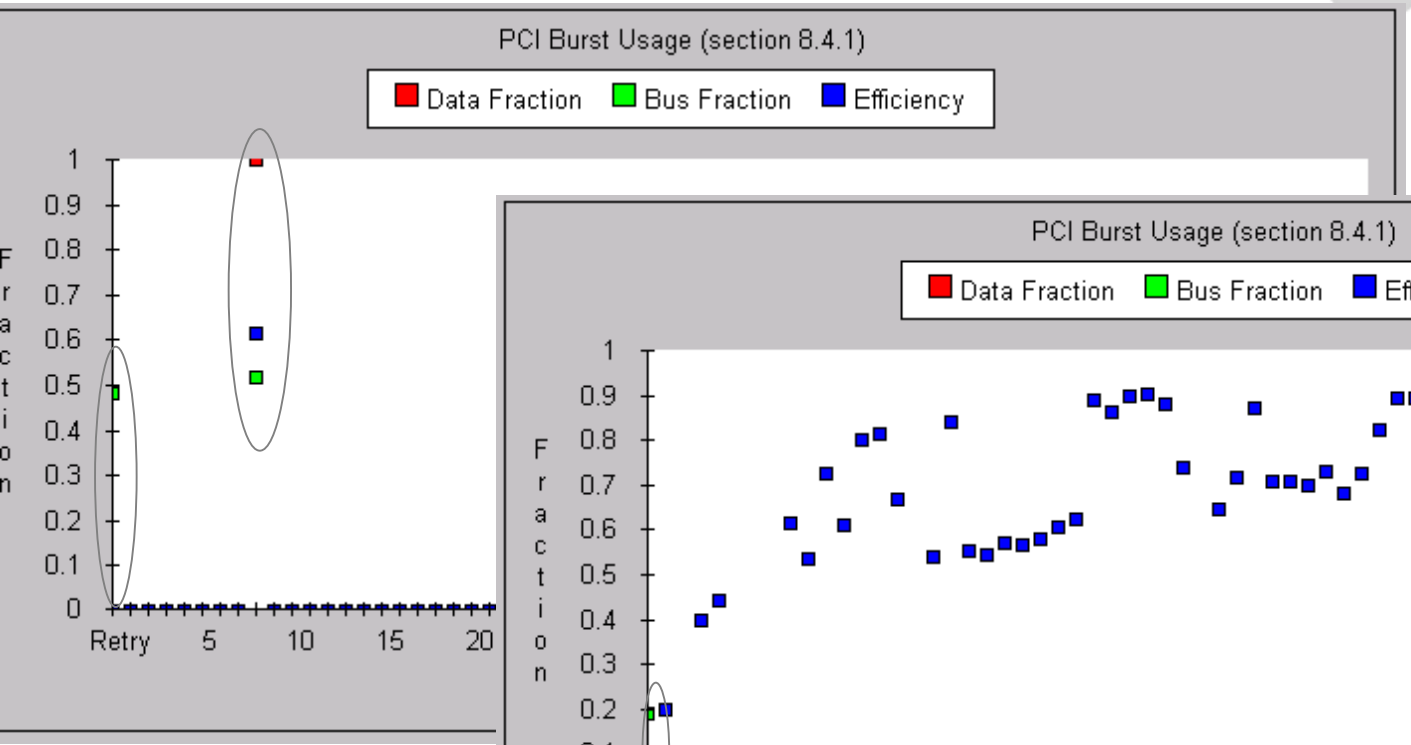
What

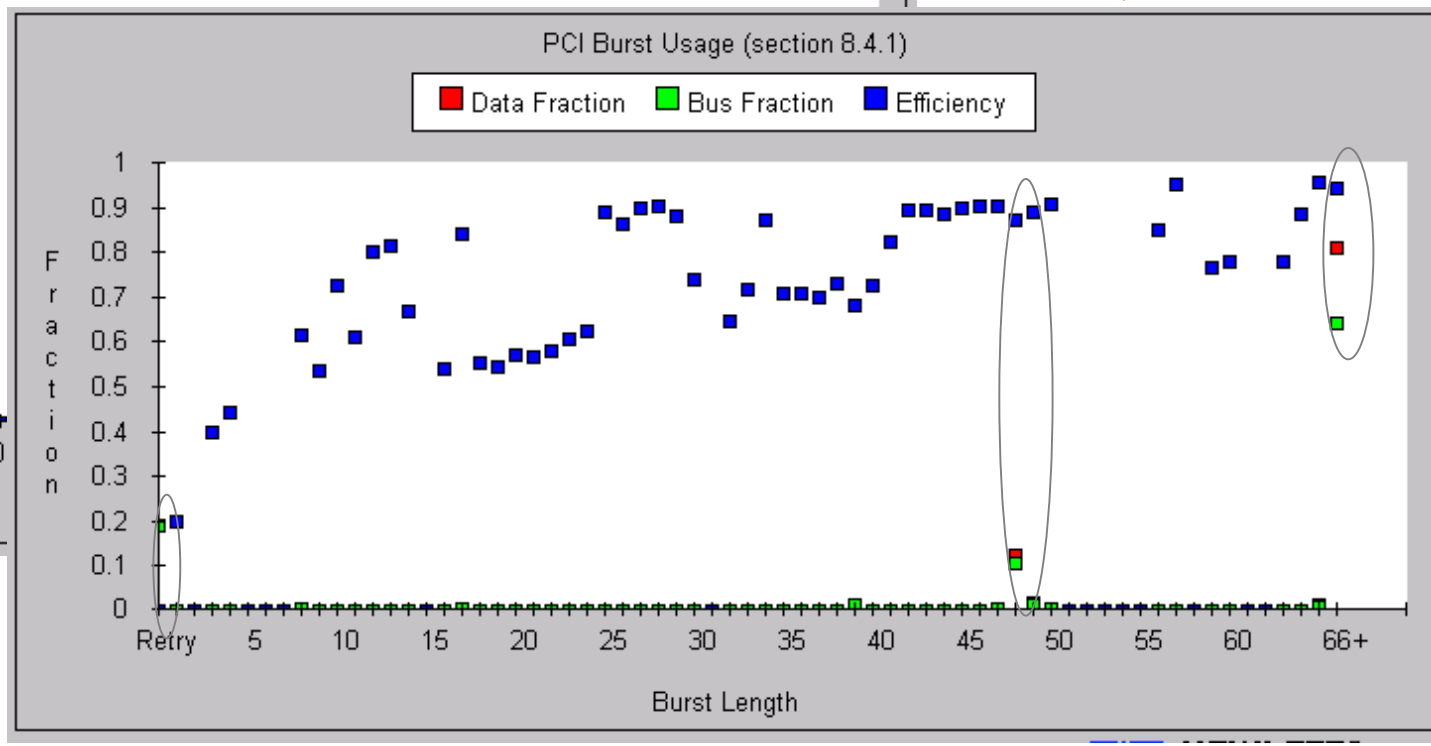
Memory Read Multiple Command



Example - Command Usage (4)

Memory Read Command - Burst Sizes





Memory Read Multiple Command - Burst Sizes

Latency Contribution

8.3.2 Time Overhead

Average Decode Speed (1 == fast).... 2.00 cycle(s)

	Overhead caused by Master	Target	Both	Sum
a) Address Phase	23.67 %	--	--	23.67 %
b) Waits	5.06 %	56.98 %	9.84 %	71.88 %
1) First Word Latency (a+b)	28.72 %	56.98 %	9.84 %	95.54 %
2) Retry Transactions	--	4.10 %	--	4.10 %
3) Subsequent Latency	0.36 %	0.00 %	0.00 %	0.36 %
Sum ((1) + (2) + (3))	29.08 %	61.08 %	9.84 %	100.00 %

Target Initial Waits

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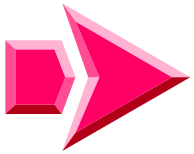

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Two ways to get performance data

- **Real Time**
  - Hardware Counters are used.
  - Values are displayed online.
  - Most measures are a ratio of two or three counter values.
  - Observation Time is very long.
- **Post Processed**
  - Values are calculated after the measure was taken.
  - Master and Target identification possible.
  - Start and end time definable by benchmark or trigger.
  - Histograms and distributions for detailed analysis can be made.

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Post Processed vs. Real Time

- **Real Time Measurements**
  - \+ precise measures over a long period of time
  - \- only very few simultaneous measures
- **Post Processed Measurements**

  - \+ deep insight knowledge of bus activity
  - \+ mandatory for improving designs
  - \- observation time is very short
  - \- maybe caught a ‘bad’ sample

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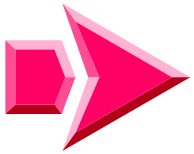

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Recommendations for Improving Device Efficiency

- **Add-In Card, Driver and Chipset Developers can improve their device efficiency by**
  - accepting bursts (and using bursts if master).
  - using the information coming out of extended commands.
  - using protocols with only minor overhead.
  - not using I/O transfers.

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Conclusions

- Efficiency is the key measurement value to determine the performance of a PCI device.
- To maximize efficiency use long bursts, use extended bus commands, use memory commands instead of IO commands and minimize latency.
- Using a standardized and hierarchical tool helps along the entire design chain from evaluating the performance of a system to optimizing chips or bridge designs and settings.

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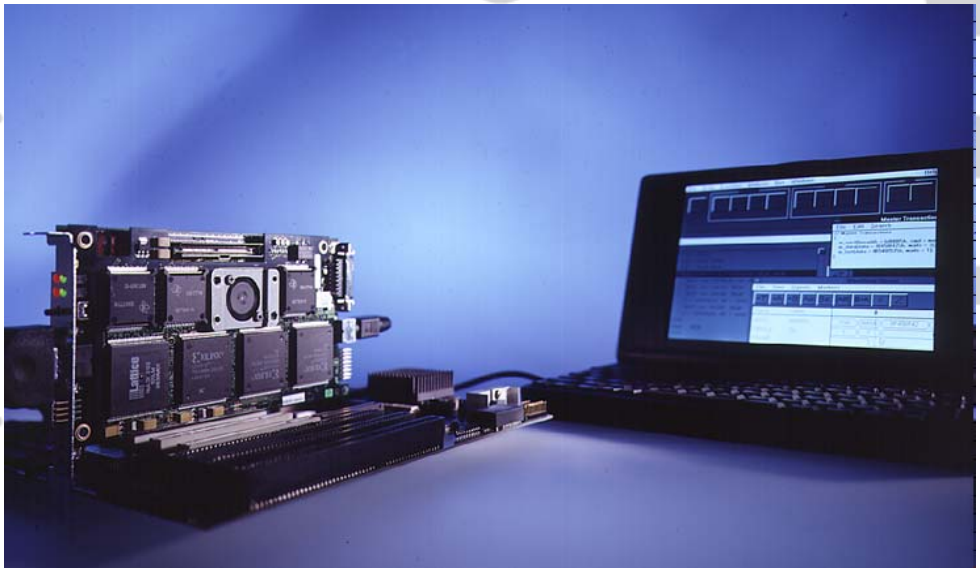
Agilent E2920 Computer Verification Tools, PCI Series

Complete Solution for the entire design cycle

- Analyzer/ Exerciser
- Performance
- System Validation
- 32/64 bit
- 33/66 MHz
- C-PCI



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